To :

Date : Jan. 11, 2018

SPECIFICATIONS	
Product Name	**LPM035M407B**

Approval Signature

Approved by	Date

Proposed by	Date

Please return **1** copy with your signature on this page for approval.

Japan Display Inc.

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RECORD OF REVISIONS

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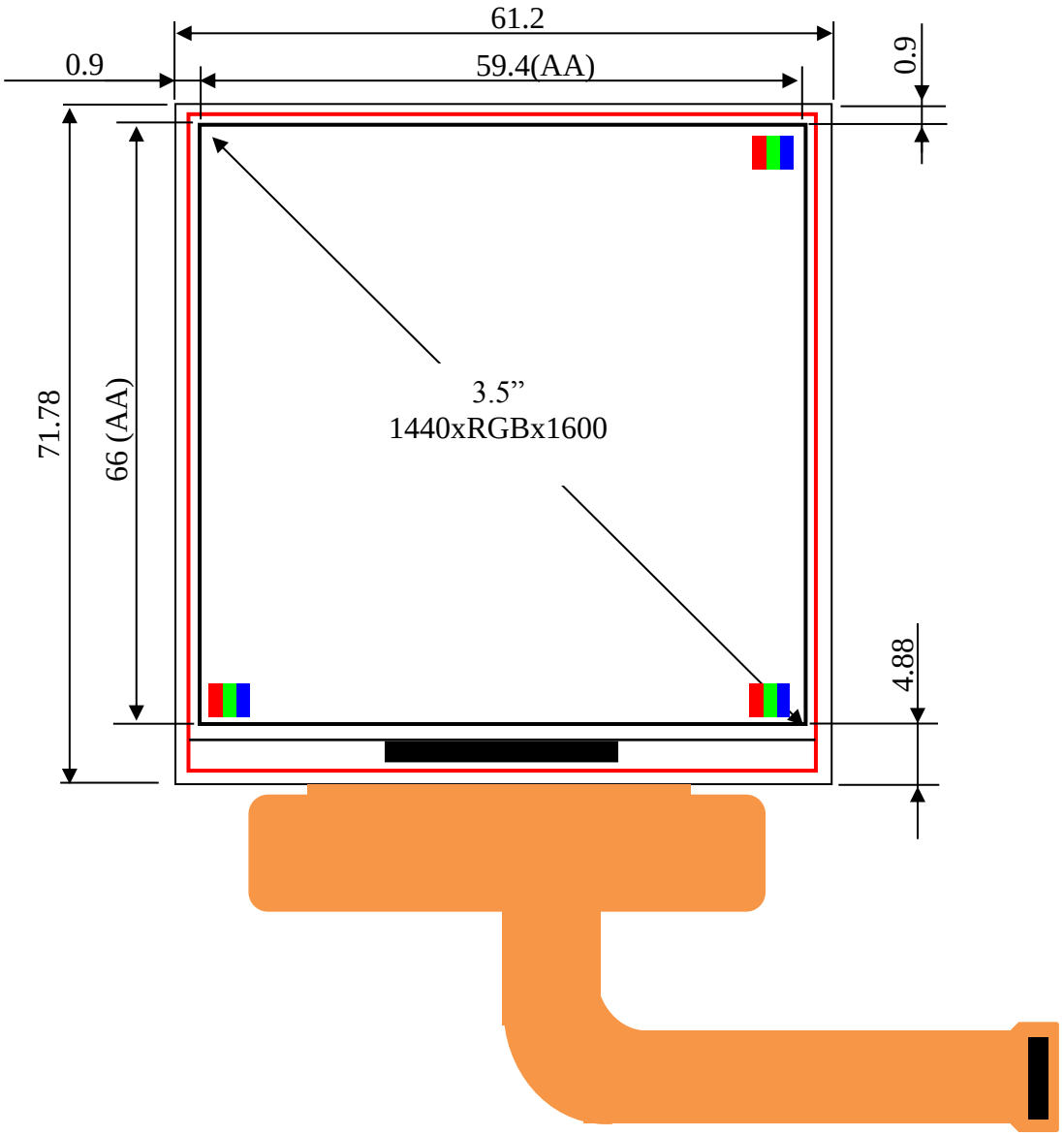
3. GENERAL DATA

(1)	Part Name	LPM035M407B
(2)	Module Dimensions	62.2 (W) mm × 73.6 (H) mm × 1.65 (t) mm (Excluding FPC and adhesive on the metal case)
(3)	Active Area Dimensions	59.4 (W) mm × 66.0 (H) mm
(4)	Pixel Pitch	0.04125 (W) mm × 0.04125 (H) mm (615ppi)
(5)	Resolution	1440 × 3 (R,G,B) (W) × 1600 (H) dots
(6)	Color Pixel Arrangement	RGB Vertical Stripe
(7)	Display Mode	Transmissive Type, Normally Black Mode, In-Plane Switching Mode
(8)	Number of Colors	16,777,216 Colors
(9)	Viewing Direction	Perpendicular to the display surface
(10)	Backlight	Light Emitting Diode (LED), 10 LEDs (2in1) ; 5 series 2 strings
(11)	Weight	17g (typ)
(12)	Power Supply Voltage	AVDD = 5.7+/- 0.1V AVEE = -5.7+/- 0.1V
(13)	Interface I/O power supply Note (1)	VDDI = 1.8V +/-0.1 V The same voltage as "H" level of a customer's interface signal must be supplied to VDDI.
(14)	IC	JD36860 (Source and Power IC : Novatek)
(15)	Interface	MIPI-DSI Video mode with data compression (4-Lane x 1-Port)
(16)	Methode of Inversion	Column Inversion
(17)	Surface Treatment	HC

Note(1) VDDI is the reference voltage for adjusting the I/O signal level of JD36860
VDDI voltage must be determined according to a customer's system.

4 LCD LAYOUT

4.1 LCD Outline



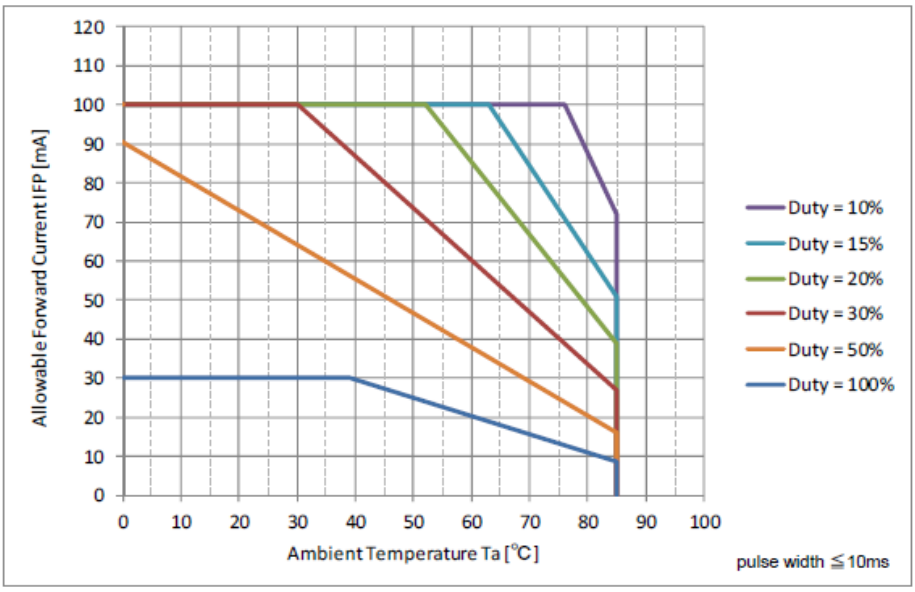
Note(1) Unspecified tolerance : ±0.2

5. ABSOLUTE MAXIMUM RATINGS

5.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD Ta=25°C

Item	Symbol	Min	Max	Unit	Note
Supply voltage	AVDD	-0.3	6.0	V	(1)
Supply Voltage	AVEE	-6.0	0.3	V	(2)
Logic Input voltage range	VDDI	-0.3	2.0	V	(1)
Supply current	AVDD	150	200	mA	
Supply current	AVEE	150	200	mA	
Logic Input current range	VDDI	300	530	mA	
MIPI line voltage range		-0.05	1.35	V	(1)
RESET voltage range		-0.3	VDDI+0.3	V	(1)
LED Reverse Voltage	V_R	-	5	V	
LED Forward Current	I_{LED}	-	Note (3)	mA	per LED

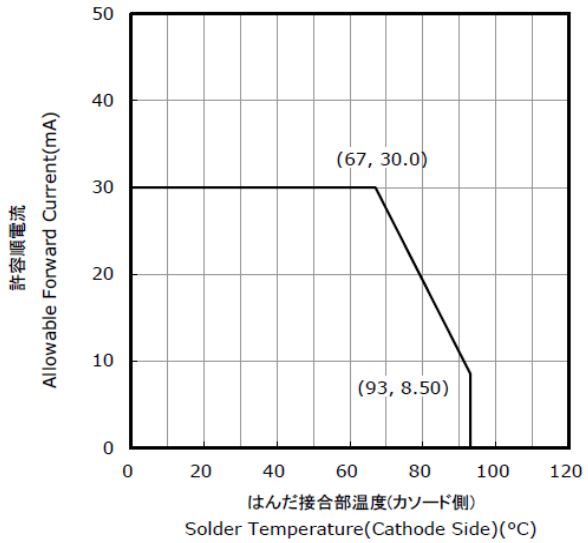
Notes (1) Keep AVDD, VDDI, MIPI line and RESET Voltages no lower than GND.
(2) Keep AVEE Voltages no Higher than GND.
(3) Ambient Temperatures vs. Allowable Forward Current.



	Ta [°C]	IFP [mA]
Duty = 10%	76	100
	85	72
Duty = 15%	63	100
	85	51
Duty = 20%	52	100
	85	39
Duty = 30%	30	100
	85	27
Duty = 50%	−11	100
	85	16
Duty = 100%	39	30
	85	8.5

In case of "pulse width ＞10ms", please apply "Duty = 100%".
パルス幅が10msを超える場合、Duty = 100%を適用下さい。

Solder Temperature(Cathode Side) vs Allowable Forward Current

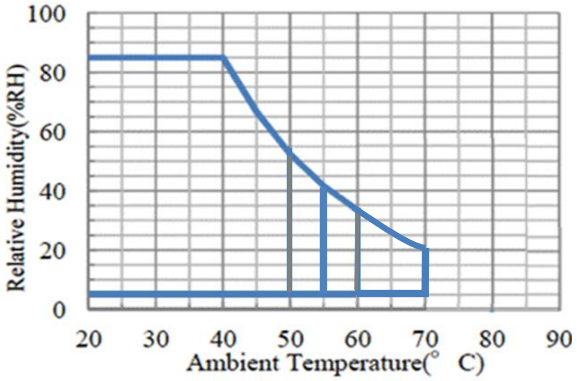


5.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Non-Operating (Note3)		Remarks
	Min	Max	Min	Max	
Ambient Temperature	-10°C	55°C	-20°C	70°C	Note (2)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta ≤ 40°C 85%RH max.

Ta > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.



(2) Background color slightly changes depending on ambient temperature and viewing angle.
The temperature for operating in the table above apply to operation only.
Visual qualities, such as contrast ratio and response time, to be evaluated at Ta=25°C Operating.

(3) This is not for storing condition. When storing LCM for long term, please follow the condition mentioned in "12.5 STORAGE".

6. ELECTRICAL CHARACTERISTICS

LCD Module Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage for LCD	VDDI	-	1.7	1.8	1.9	V	-
Power Supply Voltage for	AVDD	-	5.6	5.7	5.8	V	-
Power Supply Voltage for	AVEE	-	-5.8	-5.7	-5.6	V	-
Input Voltage for Logic Circuits	VIH		0.8×VDDI	-	VDDI	V	(1),(2)
	VIL		0	-	0.2×VDDI		
Output Voltage for Logic Circuits	VOH1	IOH=-0.1mA	0.8×VDDI	-	-	V	(1),(3)
	VOL1	IOL=0.1mA	-	-	0.2×VDDI		
Power Supply Current	I_VDDI	All White	-	62.8	92	mA	(4)
	I_AVDD	All White	-	10.5	18	mA	(4)
	I_AVEE	All White	-16	-9	-	mA	(4)
LED Forward Voltage	VLED	-	-	6.14	6.44	V	(5)
LED Forward Current	ILED	-	-	52	TBD	mA	(5)(6)
LED Reverse Current	IR	-	-	-	TBD	μA	
Frame Frequency	fFLM	-		90		Hz	

Notes (1) VDDI = 1.7V to 1.9V
(2) Input : RESET
(3) Output : LEDPWM, TE
(4) VDDI=1.8V, AVDD=5.7V, AVEE=-5.7V, fFLM=90Hz
The current is time averaged value even for Maximum criteria.
(5) Each value is the characteristics of one LED. @If=40mA Duty=10%
(6) The operating current of LED and the duty ratio should be determined within the maximum rating of the temperature environmental condition.

7. OPTICAL CHARACTERISTICS

LCD (BACKLIGHT ON)

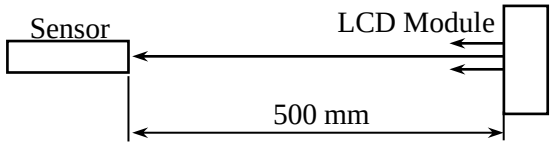
Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Brightness		B	φ=0°, θ=0°	120	150	-	cd/m^2	(1),(2)
Brightness Uniformity		-	φ=0°, θ=0°	75	85	-	%	(2),(3),(5)
Viewing Angle		CR	φ=60°, θ=0°	55	60	-	-	(4),(6),(7)
			φ=60°, θ=90°	55	60	-		
			φ=60°, θ=45°	55	60	-		
Contrast Ratio		CR	φ=0°, θ=0°	500	700	-	-	(6)
Response Time		tr+tf	φ=0°, θ=0°	5			ms	(8)
Color Tone (Primary Color)	Red	x	φ=0°, θ=0°	0.630	0.660	0.690	-	(9)
		y		0.297	0.327	0.357		
	Green	x		0.245	0.275	0.305		
		y		0.622	0.652	0.682		
	Blue	x		0.125	0.155	0.185		
		y		0.026	0.056	0.086		
	White	x		0.279	0.299	0.319		
		y		0.295	0.315	0.335		
NTSC Ratio		-		80	85	-	%	-

All the criteria shall be applied for initial(delivered) state. (Not for whole the product life.)

Measurement Conditions

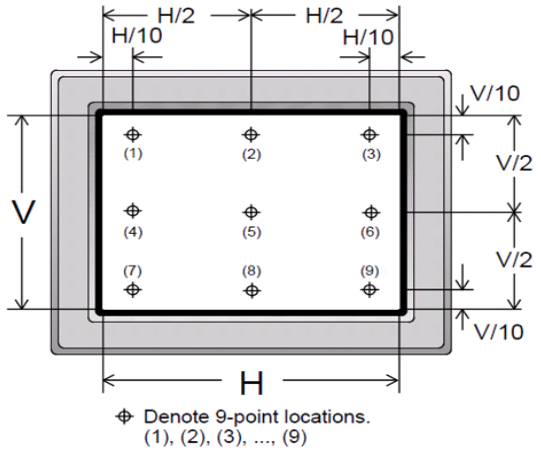
Measurement environment : Dark room
Ambient temperature : Ta=25°C
Sequence : Refer to Item 9.4
Power supply voltage : VDDI=1.8V, AVDD=5.7V, AVEE=-5.7V
Backlight current : I_{LED}=40mA x 2 Strings Duty10%

Notes (1) Display image for measurement : All White
(2) Measurment system;

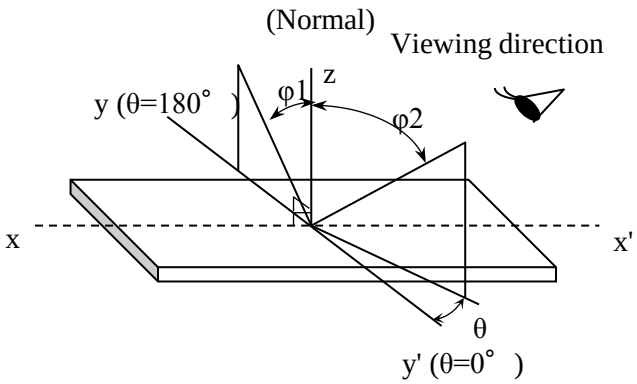


Sensor : CS-1000 or equivalent
Measurement point : Center of LCD's active area

Notes (3) Measurement point



(4) Definition of θ and φ



(5) Definition of brightness uniformity

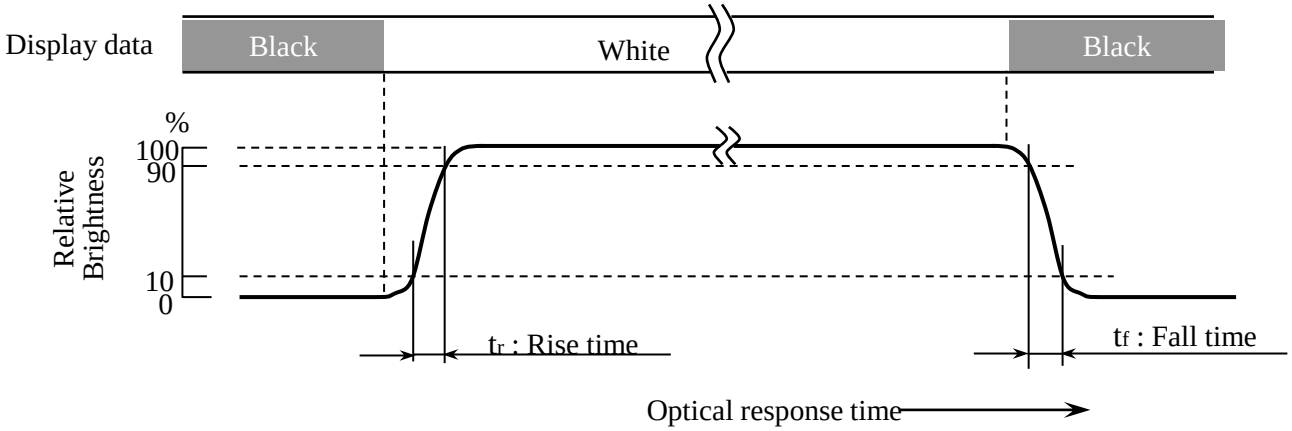
$$\text{Brightness uniformity} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\ (\%)$$

(6) Definition of Contrast "CR"

$$\text{CR} = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

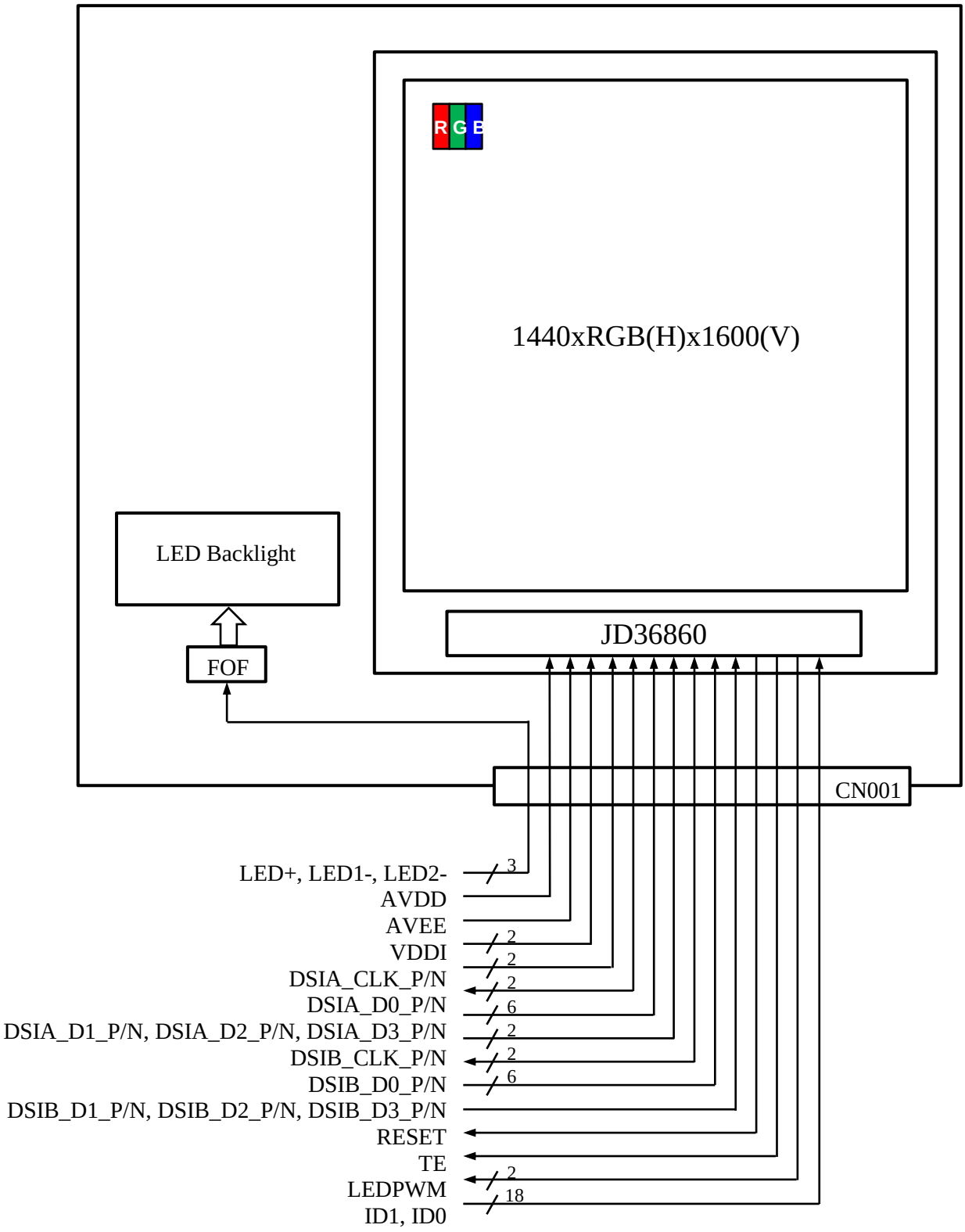
(7) Equipment Sensor : TOPCON's BM-5A or equivalent

(8) Definition of Optical Response Time

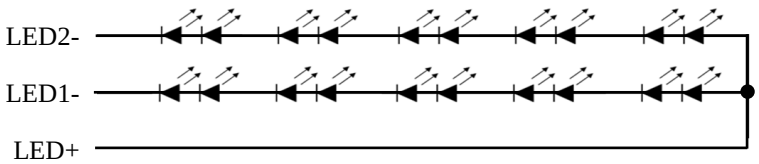


(9) It is not the guaranteed value for lot acceptance.

8. BLOCK DIAGRAM



Note 1 LED Backlight Circuit Diagram

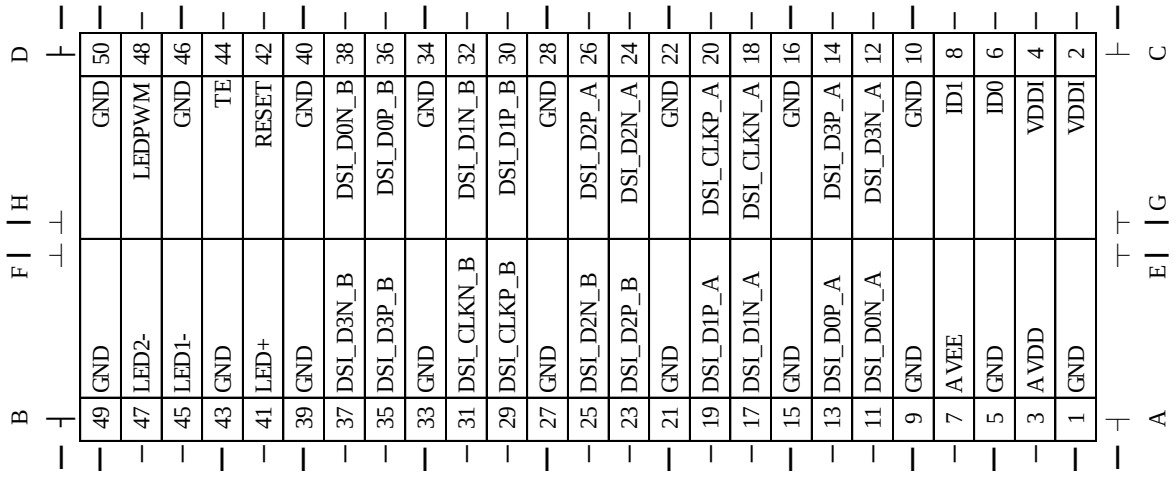


9. INTERFACE

9.1 INTERNAL PIN CONNECTION

Symbol	Pin No.		Description	Spec.
GND	1,5,9,10,15,16,21, 22,27,28,33,34,39, 40,43,46,49,50, A,B,C,D,E,F,G,H	P	Ground	
AVDD	3	P	Analog Power Supply	5.7+/-0.1V
AVEE	7	P	Analog Power Supply	-5.7+/-0.1V
VDDI	2,4	P	Logic and IF Power Supply	1.8+/-0.1V
LED+	41	P	Backlight Anode	
LED1-	45	P	Backlight Cathode	
LED2-	47	P	Backlight Cathode	
RESET	42	I	Reset fot LCD	VDDI-GND input
TE	44	O		
LEDPWM	48	O		
DSI_D0P_A, DSI_D0N_A	11,13	IO	MIPI data lane for Prot A	<1Gbps
DSI_D1P_A, DSI_D1N_A	17,19	I	MIPI data lane for Prot A	<1Gbps
DSI_D2P_A, DSI_D2N_A	24,26	I	MIPI data lane for Prot A	<1Gbps
DSI_D3P_A, DSI_D3N_A	12,14	I	MIPI data lane for Prot A	<1Gbps
DSI_D0P_B, DSI_D0N_B	36,38	IO	MIPI data lane for Prot B	<1Gbps
DSI_D1P_B, DSI_D1N_B	30,32	I	MIPI data lane for Prot B	<1Gbps
DSI_D2P_B, DSI_D2N_B	23,25	I	MIPI data lane for Prot B	<1Gbps
DSI_D3P_B, DSI_D3N_B	35,37	I	MIPI data lane for Prot B	<1Gbps
DSI_CLKP_A, DSI_CLKN_A	18,20	I	MIPI clock lane for Prot A	<1Gbps
DSI_CLKP_B, DSI_CLKN_B	29,31	I	MIPI clock lane for Prot B	<1Gbps
ID1, ID0	6,8	O	ID(Ground)	

KYOCERA Connector producuts Corporation
14 5863 050 024 829+ BtoB(Plug)
CN001 50pin



9.2 TIMING CHARACTERISTICS

(1)MIPI DSI Characteristics

Item		Symbol	Unit	Condition	Min	Typ	Max	Note
HS-RX	Differential input high threshold	VIDTH	mV	VDDI=1.65~1.95V	-	-	70	
	Differential input low threshold	VIDTL	mV	VDDI=1.65~1.95V	-70	-	-	
	Single-ended input low voltage	VILHS	mV	VDDI=1.65~1.95V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	VDDI=1.65~1.95V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	VDDI=1.65~1.95V	70	-	330	
	Differential input impedance	ZID	Ω	VDDI=1.65~1.95V	80	100	125	
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	VDDI=1.65~1.95V	-	-	550	
	Logic 1 input voltage	VIH	mV	VDDI=1.65~1.95V	880	-	-	
LP-TX	Thevenin output low level	VOL	mV	VDDI=1.65~1.95V	-50	-	50	
	Thevenin output high level	VOH	V	VDDI=1.65~1.95V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	VDDI=1.65~1.95V	80	100	125	
CD-RX	Logic 0 contention threshold	VILCD	mV	VDDI=1.65~1.95V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	VDDI=1.65~1.95V	450	-	-	

MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
UI instantaneous	UI_{INST}	ns	VDDI=1.65~1.95V	1	-	4	1, 2, 7
Data to Clock Skew [measured at transmitter]	T_{SKEW} [TX]	UI_{INST}	VDDI=1.65~1.95V	-0.15	-	0.15	3
Data to Clock Setup Time [measured at receiver]	T_{SETUP} [RX]	UI_{INST}	VDDI=1.65~1.95V	0.15	-	0.15	4
Data to Clock Hold Time [measured at receiver]	T_{HOLD} [RX]	UI_{INST}	VDDI=1.65~1.95V	0.15	-	0.15	4
20% - 80% rise time and fall time	t_R / t_F	ps	VDDI=1.65~1.95V	150	-	-	6
		UI_{INST}	VDDI=1.65~1.95V	-	-	0.3	5

Notes 1. This value corresponds to a minimum 250 Mbps data rate.

2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

3. Total silicon and package delay budget of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps.

4. Total setup and hole window for receiver of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps.

5. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).

6. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

7. For MIPI speed limitation:

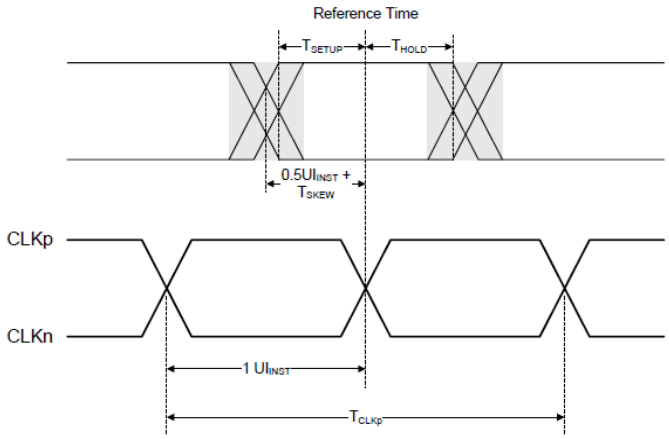
[1] Per lane bandwidth is 1Gbps,

[2] Total Bit Rate: 4Gbps for 8-8-8; 2.67 Gbps for 6-6-6; and for5-6-5.

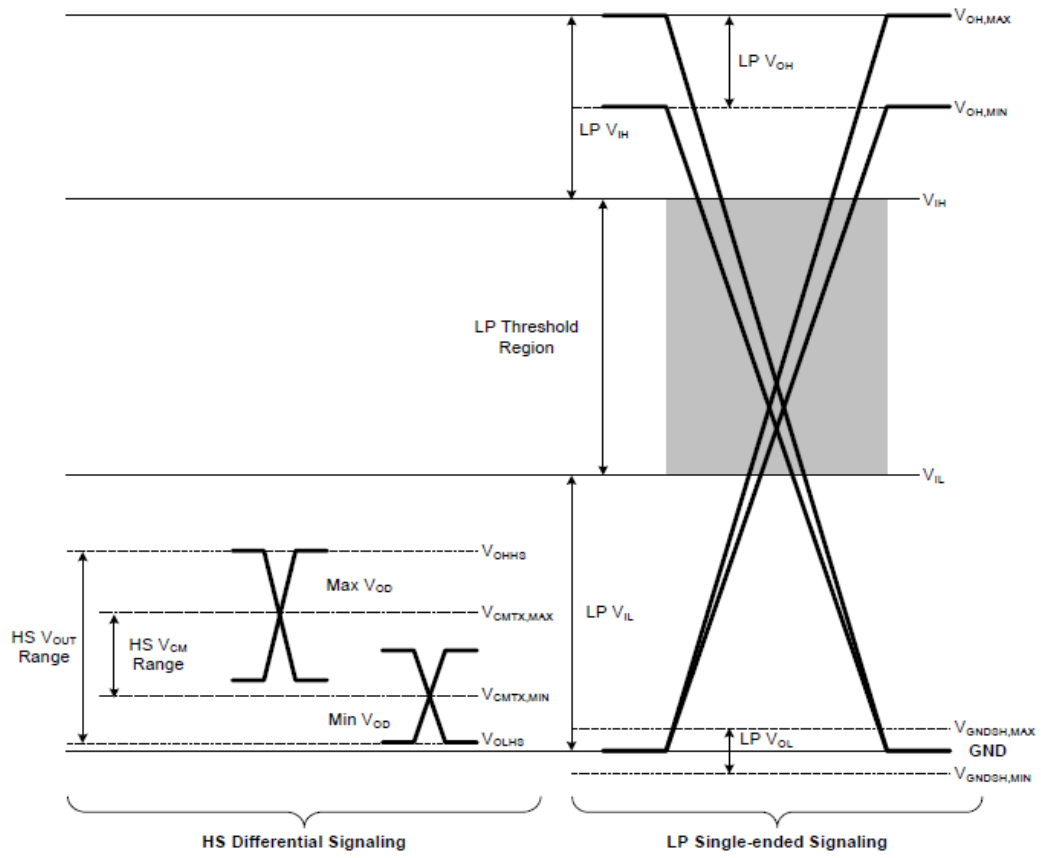
MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		VDDI=1.65~1.95V	40ns +4*UI	-	85ns +6*UI	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$		VDDI=1.65~1.95V	60ns + 4*UI	-	-	
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	ns	VDDI=1.65~1.95V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		VDDI=1.65~1.95V	$4*T_{LPX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		VDDI=1.65~1.95V	$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}		VDDI=1.65~1.95V	$5*T_{LPX}$			
Length of any Low-Power state period	TLPTX	ns	VDDI=1.65~1.95V	50	-	-	
Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		VDDI=1.65~1.95V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$		VDDI=1.65~1.95V	60ns +52UI	-	-	
$T_{CLK-PREPARE}$ + Time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	ns	VDDI=1.65~1.95V	300	-	-	

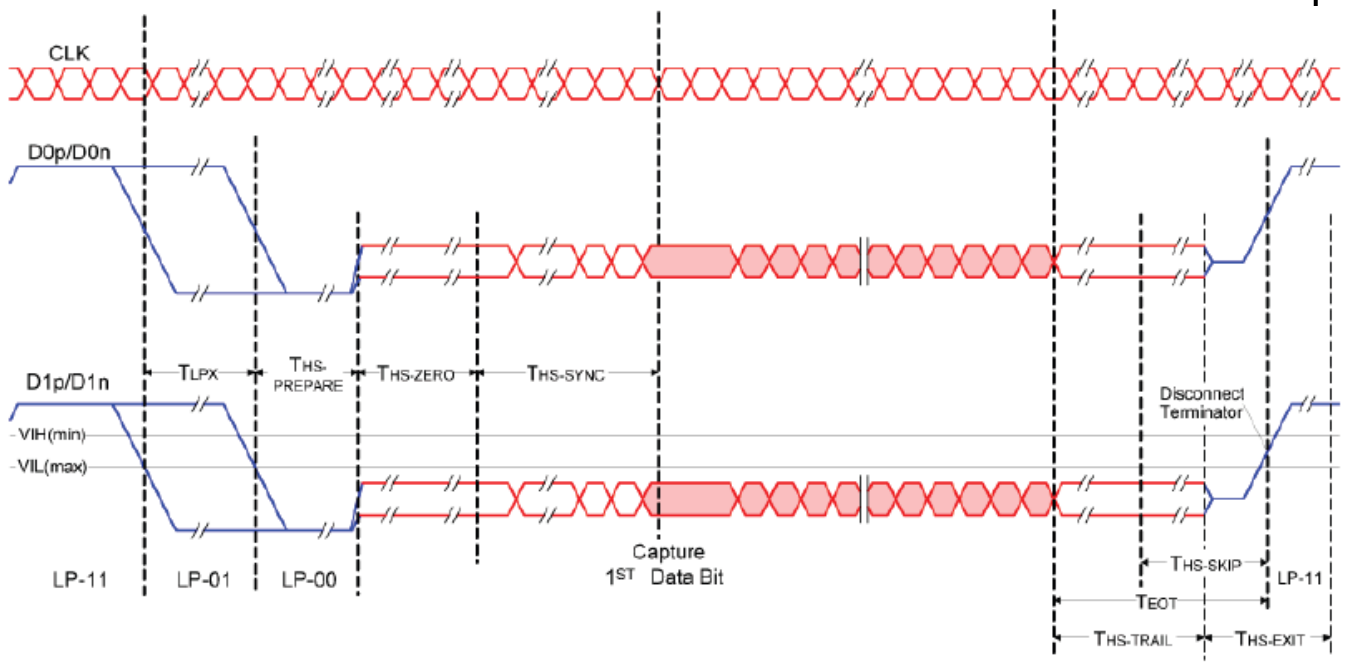
Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	VDDI=DPHYVCC =1.65~1.95V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	VDDI=DPHYVCC =1.65~1.95V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	VDDI=DPHYVCC =1.65~1.95V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		VDDI=DPHYVCC =1.65~1.95V	-	-	105ns + 12*UI	



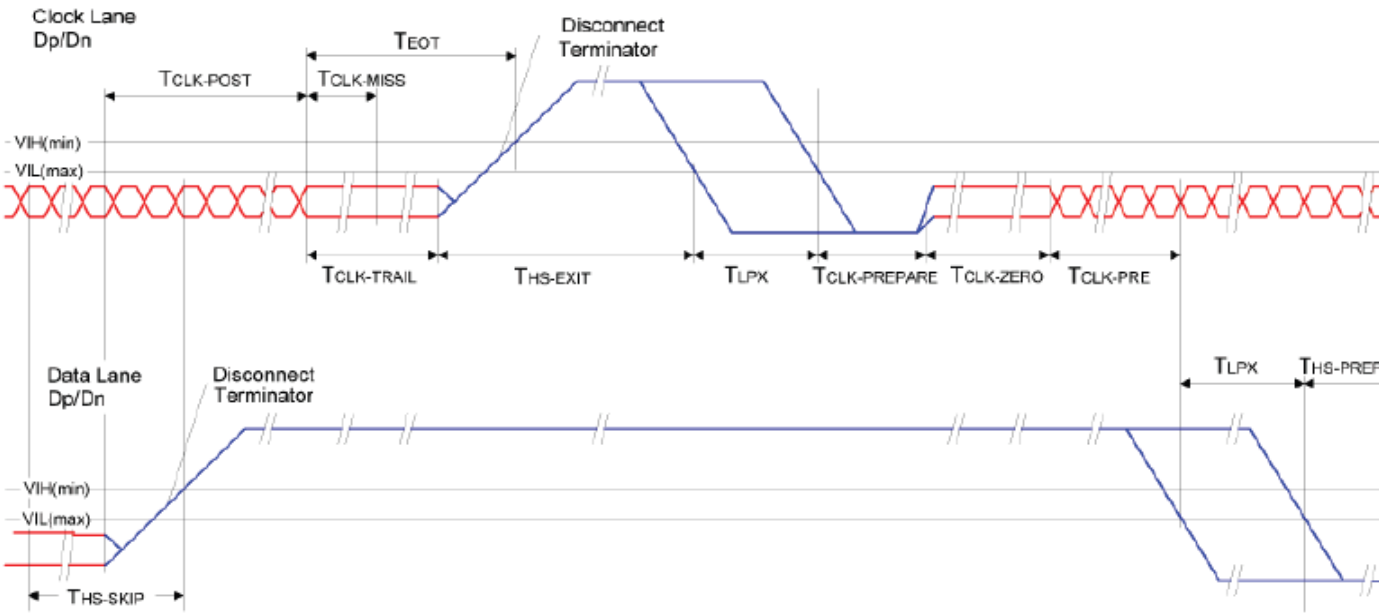
Data to Clock Timing Definitions

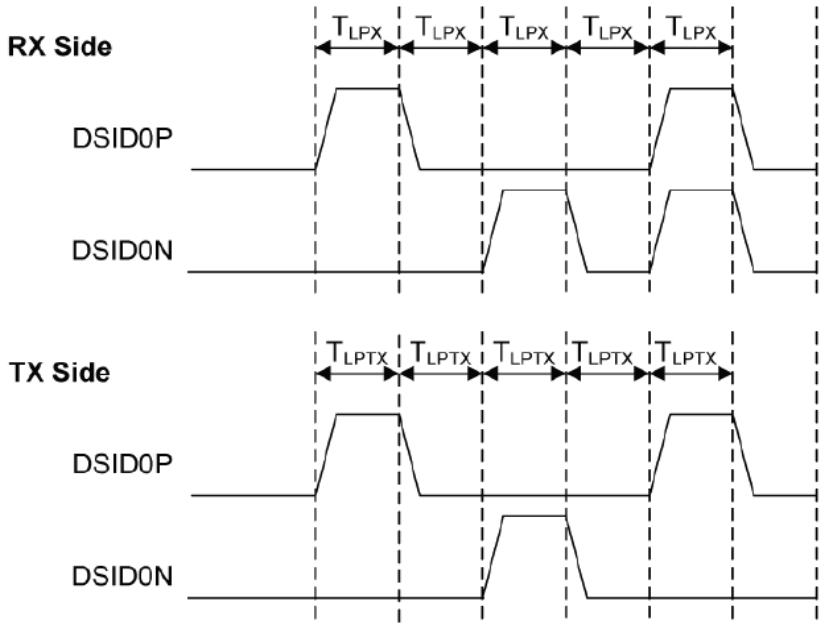


D-PHY Signaling Levels



Note: THS-SYNC: Proper match found for Sync sequence in HS stream,the following bits are payload data.





Video timing for non-compression mode

MIPI Video Mode Timing

Compression intrface 4-lane x 1-port

	min	typ	max	unit
MIPI DSI			1000	Mbps/lane
Frame Rate (Host side)			90	Hz
Vertical Front Porch		150		Lines
Vertical Back Porch		150		Lines
Active line per frame		1600		Lines
Line Time	5.85			us
Horizontal back porch	0.16			us
Horizontal front porch	0.416			us

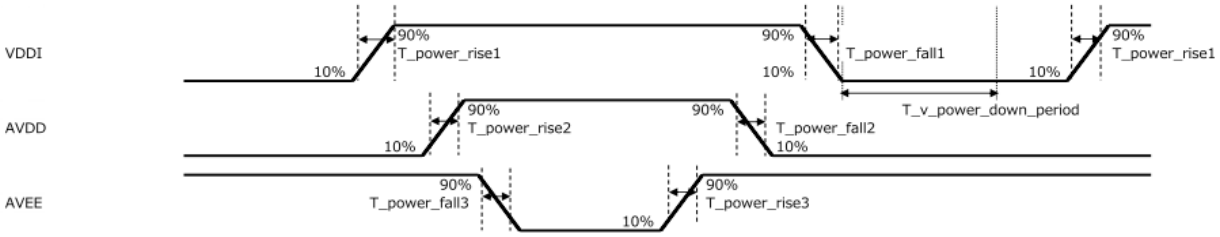
9.3 POWER ON/OFF SEQUENCE

1. Supply Power Voltage

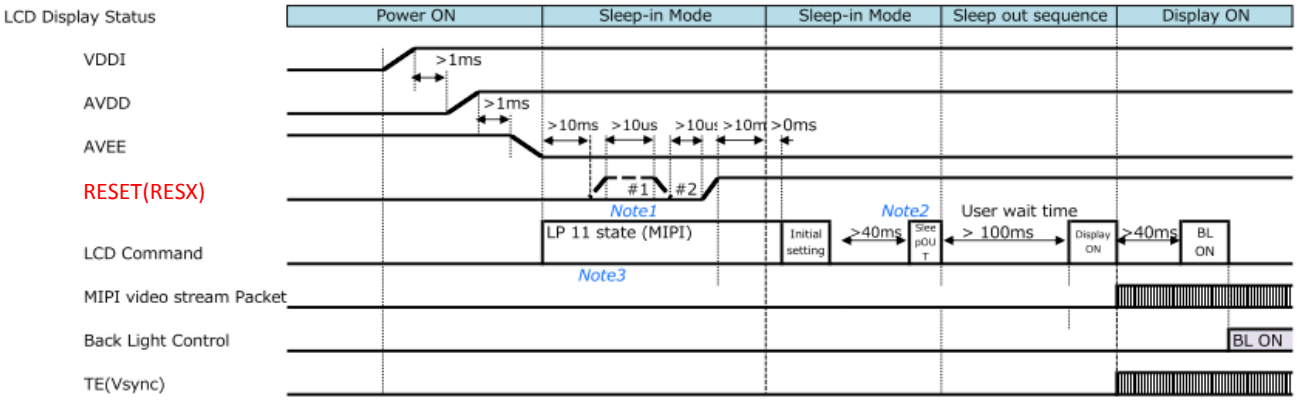
	Min	Typ	Max	Description
AVDD	5.6	5.7	5.8	Analog power supply for LCD.
AVEE	-5.8	-5.7	-5.6	Analog power supply for LCD.
VDDI	1.7	1.8	1.9	Digital power supply for LCD and TP.

2. Supply Power Slew rate

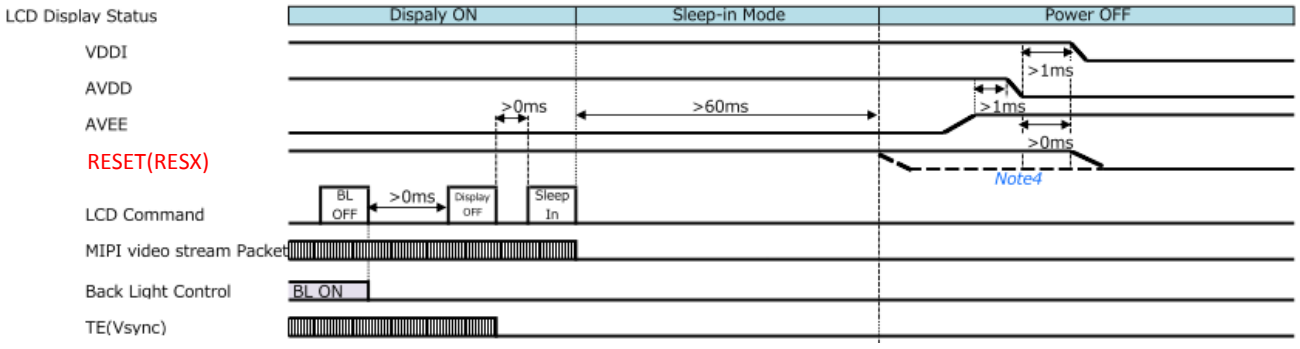
	Min	Typ	Max	Description
T_power_rise1	-	-	2ms	
T_power_fall1	-	-	2ms	
T_power_rise2	0.2ms	-	5ms	
T_power_fall2	0.2ms	-	5ms	
T_power_rise3	0.2ms	-	5ms	
T_power_fall3	0.2ms	-	5ms	
T_V_power_down_period	10ms	-	-	



3. Power On sequence



4. Power Off sequence



Note 1: The RESET waveform #1(rise-fall-rise) is better thean #2(one rise)
Note 2: After Sleep-Out command, Driver IC will reload MTP registers and do internal power on action.
Therefore, any initial setting by MIPI should be set
after Sleep-Out command with minimum delay time 100ms.
Note 3: When use MIPI lanes must go to LP11 state during power-on and RESET sequence

9.4 SEQUENCE

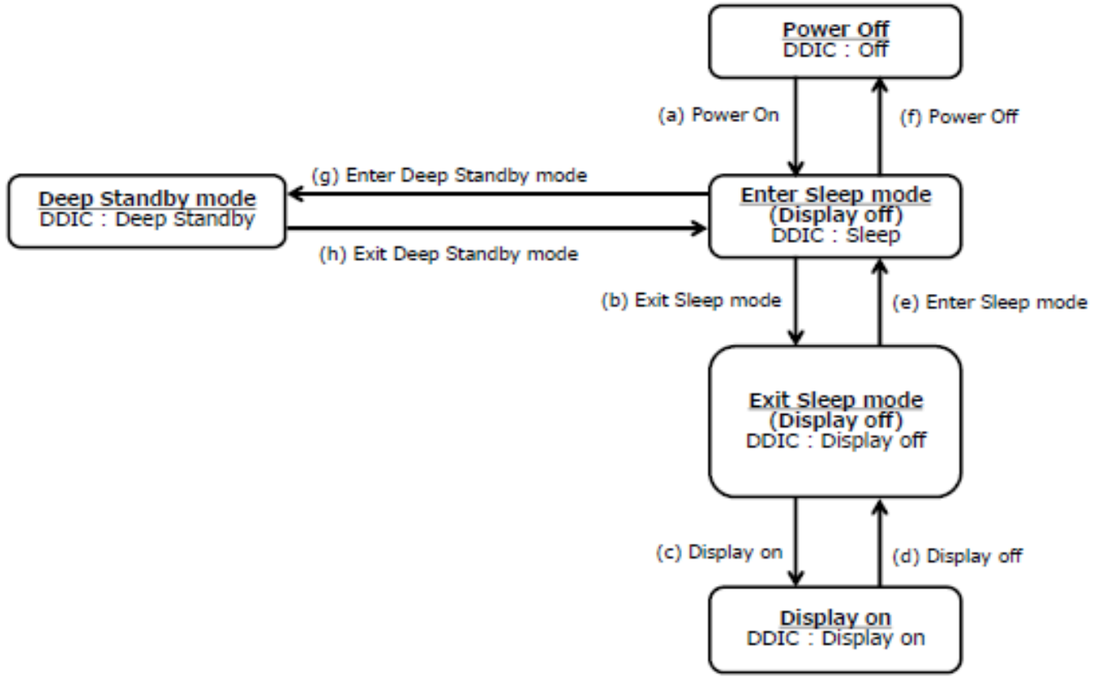
Power On Sequence

(a) Power On Sequence

Step	Action/Command
1	Reset="L"
2	VDDI On
3	Wait 1ms (min.)
4	AVDD On
5	Wait 1ms (min.)
6	AVEE On
7	Wait 10ms (min.)
8	Reset="H"
9	Wait 10us (min.)
10	Reset="L"
11	Wait 10us (min.)
12	Reset="H"
	Wait 10ms (min.)

State transition diagram

State Transition Diagram



9.4 SEQUENCE

Initial setting & exit sleep mode sequence for non-compression mode

(b) Exit Sleep mode Sequence (Initial setting & Exit Sleep mode)

For mipi video mode

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	Page select	DCS	15	0xFF	0x10					
2	Reload	DCS	15	0xFB	0x01					
3	SET_HORIZONTAL_ADDRESS	DCS	39	0x2A	0x00					
					0x00					
					0x05					
					0x9F					
4	SET_VERTICAL_ADDRESS	DCS	39	0x2B	0x00					
					0x00					
					0x06					1600
					0x3F					
5	SET_TEAR_ON	DCS	15	0x35	0x00					
6	SET_MIPI_LANE	DCS	15	0xBA	0x07					4-lane x 1-port
7	SETDSIMODE	DCS	15	0xBB	0x13					03: Video Mode bypass RAM, 10: Command Mode, 13: Video Mode with RAM
8	BK_EN	DCS	15	0xE5	0x00					Random 00h, Black 01h
9	Page select	DCS	15	0xFF	0x26					PWM adjustment for JDI recommended video timing
10	Reload	DCS	15	0xFB	0x01					
11	DELY_VID	DCS	15	0x02	0xC0					
12	DELY_VID	DCS	15	0x03	0x00					
13	Page select	DCS	15	0xFF	0x25					
14	Reload	DCS	15	0xFB	0x01					
15	PIN CTRL3	DCS	15	0x62	0x60					
16	VSOUTS_1	DCS	15	0x65	0x00					
17	VSOUTS_2	DCS	15	0x66	0x07					
18	VSOUTW	DCS	15	0x67	0x56					10% duty
19	Page select	DCS	15	0xFF	0xD0					
20	Reload	DCS	15	0xFB	0x01					
21	Adjustment of timing	DCS	15	0x05	0x88					
22	Page select	DCS	15	0xFF	0x10					
23	Reload	DCS	15	0xFB	0x01					
24	Compression	DCS	15	0xC0	0x83					VESA DSC High Frame Rate Mode enable
25	RGBMIPICTRL_HF	DCS	39	0xBE	0x01					
					0x90					
					0x0F					
					0x39					
26	exit_sleep_mode	DCS	05	0x11	-					
27	Wait 100ms (min.)									

(c) Display on Sequence

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	SET_DISPLAY_ON	DCS	05	0x29						
2	**Video Image Start**									
3	Wait 40ms (min.)									

(d)Display off Sequence

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	SET_DISPLAY_OFF	DCS	05	0x28						

(e) Enter Sleep mode Sequence

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	SET_TEAR_OFF	DCS	05	0x34						
2	ENTER_SLEEP_MODE	DCS	05	0x10						

(f) Power Off Sequence

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	Reset="L"									
2	Wait 1ms(min.)									
3	AVEE Off									
4	Wait 1ms(min.)									
5	AVDD Off									
6	Wait 1ms(min.)									
7	VDDI Off									

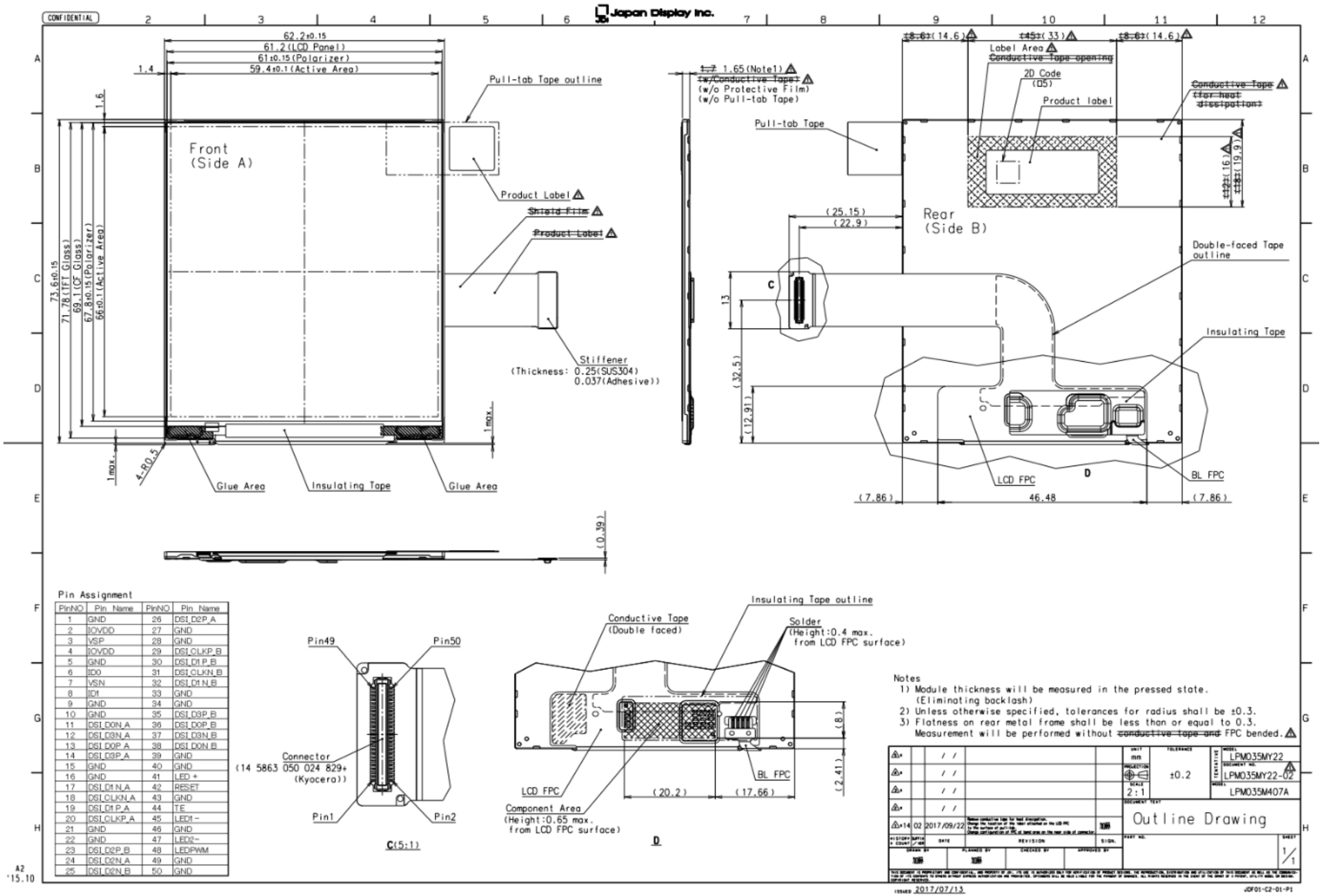
(g) Enter Deep Standby mode Sequence

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	ENTER_DSTB_MODE	DCS	15	0x4F	0x01					
2	Enter ULPM									All Mipi lanes should be VSS with specified sequence in MIPI like as below. • Start: LP-11 • Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00 • Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit) • Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

(h) Exit Deep Standby mode Sequence(1)

Step	Action/Command	DSI Data Type		Address	Data	I2C Address (TP)	Param 1	Param 2	Param 3	Note
1	Reset="L"									
2	Wait 3ms (min.)									
3	Exit ULPM									All Mipi laes should be 1.2V with specified sequence in MIPI like as below. • Mark-1: LP-00 =>LP-10 =>LP-11
4	Wait 10ms (min.)									

10. DIMENSIONAL OUTLINE



Pin Assignment

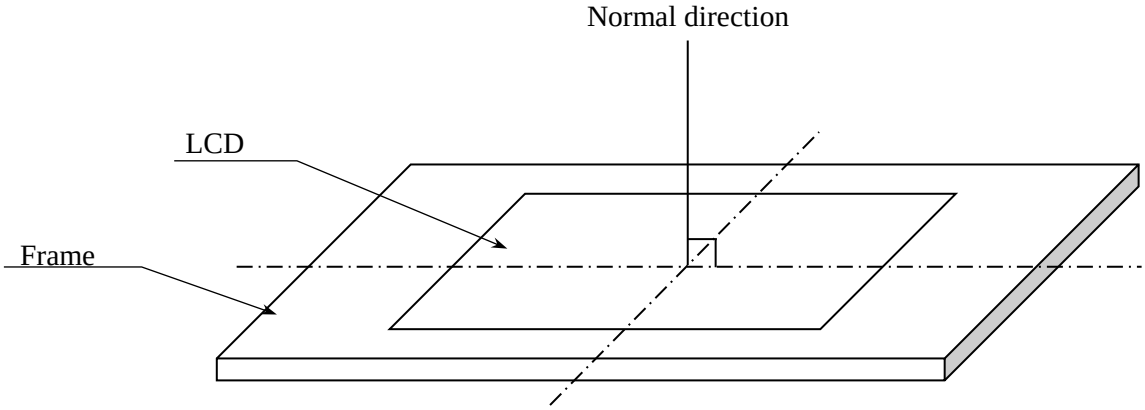
PinNO	Pin Name	PinNO	Pin Name
1	GND	26	DSI_D2P_A
2	IOVDD	27	GND
3	VSP	28	GND
4	IOVDD	29	DSI_CLKP_B
5	GND	30	DSI_D1P_B
6	ID0	31	DSI_CLKN_B
7	VSN	32	DSI_D1N_B
8	ID1	33	GND
9	GND	34	GND
10	GND	35	DSI_D3P_B
11	DSI_D0N_A	36	DSI_D0P_B
12	DSI_D3N_A	37	DSI_D3N_B
13	DSI_D0P_A	38	DSI_D0N_B
14	DSI_D3P_A	39	GND
15	GND	40	GND
16	GND	41	LED +
17	DSI_D1N_A	42	RESET
18	DSI_CLKN_A	43	GND
19	DSI_D1P_A	44	TE
20	DSI_CLKP_A	45	LED1 −
21	GND	46	GND
22	GND	47	LED2−
23	DSI_D2P_B	48	LEDPWM
24	DSI_D2N_A	49	GND
25	DSI_D2N_B	50	GND

11. VISUAL INSPECTION

11.1 INSPECTION CONDITION

(1) Ambient illumination 1 : 0 - 40[lx] for B/L ON item
(2) Ambient illumination 2 : 1000 - 1200 [lx] for B/L OFF item
(3) Distance between inspector's eyes and LCD Module : Approximately 20 [cm]
(4) Viewing angle : 0° (Normal direction)
(5) Ambient Temperature : 25°C

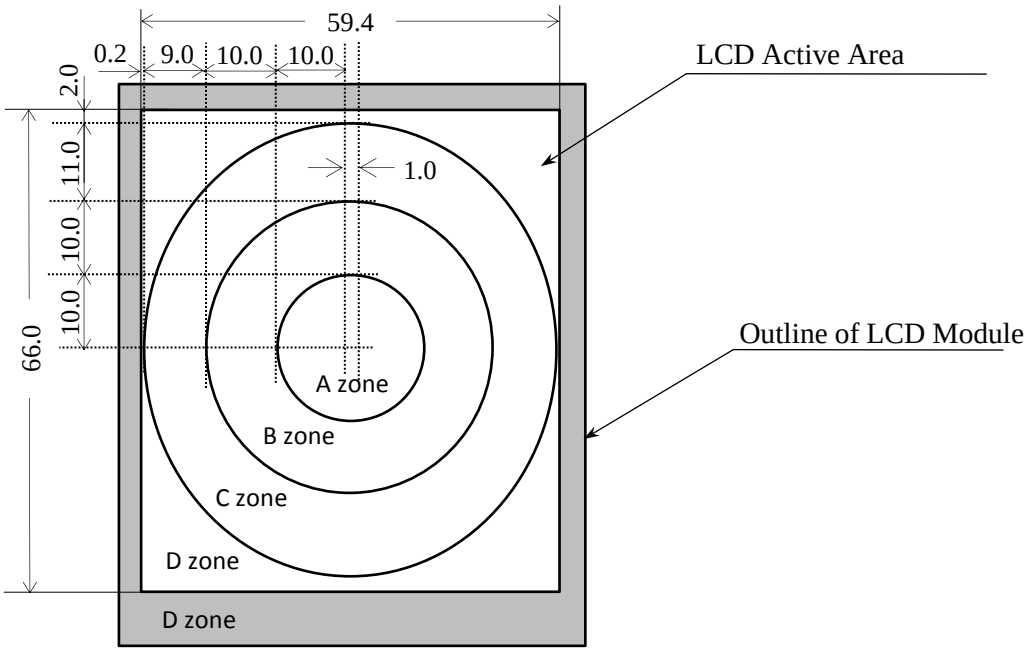
Refer to the Measurement Conditions described in Item 6 for the conditions other than specified here.



11.2 DEFINITION OF ZONE

The visual inspection zones of LCD Module is divided into four as follows.

A zone : Inspection area for VR Active Area A
B zone : Inspection area for VR Active Area B
C zone : Inspection area for VR Active Area C
D zone : Whole LCD module except A, B and C zone (Including FPC and frame)

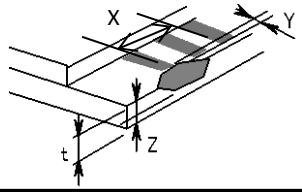
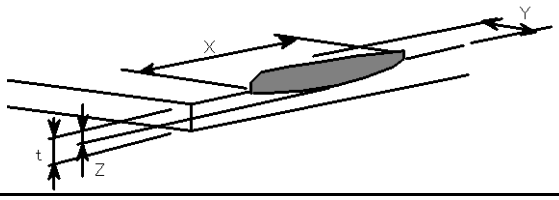
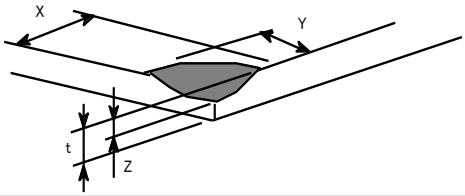


11.3 COSMETIC SPECIFICATION

11.3.1 Screen Defects Specification for LCD Module

No.	Item				Maximum Acceptable Number	Unit	Applied zone	LCD module	Back light	Note
1	Bright Defect (Bright Dot, Bright Foreign Particles, Stain, Scratch, Air Bubble)				Ignored	PC	D	On		(1), (2), (3)
		Defect size is larger than the Dummy White Dot of Limit Pattern			0	PC	A, B, C			
		Defect size is equal to or smaller than the Dummy White Dot of Limit Pattern, check the brightness			-	-	-			
			Brightness is Darker than Bright Defect Limit Pattern (R,G,B,W)		Ignored	PC	A, B, C			
			Brightness is equal to or Brighter than Bright Defect Limit Pattern (R,G,B,W)		0	PC	A			
					1	PC	B			
					2	PC	C			
	Dark Defect (Dark Dot, Dark Foreign Particles, Stain, Scratch, Air Bubble) D:Average diameter [mm]				Ignored	PC	D	k		(3), (4)
		Defect size is larger than the Dummy Dark Dot of Limit Pattern (L)			0	PC	A, B, C			
		Defect size is equal to or smaller than the Dummy Dark Dot of Limit Pattern (L)			2	PC	C			
			Defect size is larger than the Dummy Dark Dot of Limit Pattern (S)		0	PC	B			
			Defect size is equal to or smaller than the Dummy Dark Dot of Limit Pattern (S)		-	-	-			
				Brightness is Brighter than Dark Defect Limit Pattern	Ignored	PC	A,B			
				Brightness is equal to or Darker than Dark Defect Limit Pattern	0	PC	A			
					2	PC	B			
	Total number = Bright defect + dark defect				N<=4 , DS>=4mm	PC	A,B,C	On		-
	Line Defect				0	PC	A, B, C	On		-
	Uneven Brightness (Linear)				Serious one is not allowed	-	A, B, C	On		(6)
	Uneven Brightness (Circular)									
	Scratch of Polarizer (Liner)[mm] W:Width, L:Length	W≤0.05	L≤5		Ignored	PC	A, B, C	Off		(5), (6), (7)
			5<L		0					
		0.05<W	-		0					
	Scratch of Polarizer (Circular)[mm] D:Average diameter	D≤0.25			Ignored	PC	A, B, C	Off		(5), (6), (7)
		0.25<D			0					
		-			-					
	Air Bubble [mm] D:Average diameter	D≤0.25			Ignored	PC	A, B, C	Off		(5), (6), (7)
		0.25<D			0					
		-			-					
	Scratch of FPC				Serious one is not allowed	-	D	Off		(7)

11.3.2 Panel chipping Specification: It is internal standard, and this is not guaranteed SPEC.

Item	Criterion for Defects		Note
Glass Chipping [Pad Area]		Size (mm) X≦2.0 Y≦0.5 Z≦t	(8)
Glass Chipping [Except Pad Area]		Size (mm) X≦2.0 Y≦0.5 Z≦t	(8)
Glass Chipping [Corner]		Size (mm) X(or Y)≦1.0 Y(or X)≦2.0 Z≦t	(8)
Progressive crack is NG			(8)

Notes (1) Bright defects are judged below

Bright defect judgment pattern

Item	White	Red	Green	Blue	D(white)
Bright Defect Limit Pattern	35	60	35	88	-
Dummy White Dot of Limit Pattern	-	-	-	-	96

Display screen : Black (W0)

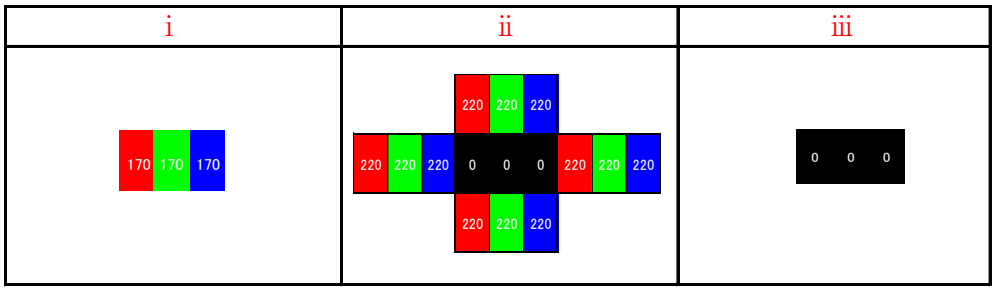
A bright defect is one that appears brighter than the bright defect limit pattern.
Those less than or equal to the brightness of the limit pattern are ignored as defects.
The defect size is judged by visual comparison with the dummy white dot pattern.

(2) Defective dots which are not adjacent are taken as a single Dot Defect each.
Two adjacent defective dots are considered as a single Dot Defect.

(3) Dark defects are judged the condition below..

Item	D(White)	Note
Dark Defect Limit Pattern	170	i
Dummy Dark Dot of Limit Pattern (L)	0 & 220	ii
Dummy Dark Dot of Limit Pattern (S)	0	iii

Display screen : White (W255)



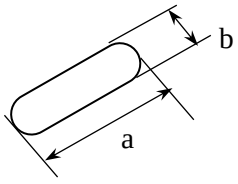
(4) Two or less bright dots are allowed if a distance is over 4 mm.

(5) Something which can be easily wiped off is disregarded as a defect.

(6) In case a problem arises, both parties should discuss needed items such as limit samples.

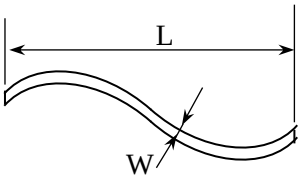
(7) Definitions for D, W and L are as follows.

Definition of D



$$D = \frac{a + b}{2} (mm)$$

Definition of W and L



(8) None reach TFT pattern.

11.4 RELIABILITY TEST

No.	Test Items	Conditions		Note
1	High temperature, operating	70℃	240h	(1), (2),
2	Low temperature, operating	-20℃	240h	
3	High temperature & high humidity, operating	60℃, 90%RH	240h	
4	High temperature, Non-operating	80℃	240h	(2)
5	Low temperature, Non-operating	-30℃	240h	
6	High temperature & high humidity, Non-operating	60℃, 90%RH	240h	
7	Thermal shock, Non-operating	-30℃ (0.5h) / +80℃ (0.5h)	50cyc	
8	Static Electricity	1. HBM IEC 61340-3-1, ESD STM5.1 C=100pF, R=1.5kohm, LCD:Non-operation V=+/-2kV (Contact discharge on I/F connector pins) V=+/-6kV (Air dischage to the center and 4-corners on the LCD's A/A) 2. IEC61000-4-2 C=150pF, R=330ohm, LCD:Operation V=+/-4kV (Contact discharge, w/Grand) V=+/-4kV (Air discharge, wo/Grand)		(2)
	Shock	100G, 6ms, +/-X, +/-Y, +/-Z, 1 time/each direction		(2)
10	Packing vibration	Random Vibration, 80min, Direction:X,Y and Z		(2), (3)
11	Packaging drop	Drop height : 80 cm, Dropping the package on 1 corner, 3 edges, 6 surfaces, once each.		(2), (3)

Notes

(1) Operation conditions : VDDI=1.8V, AVDD=5.7V, AVEE=-5.7V, fFLM=90Hz.

(2) To be no defective functions related to electrical and/or optical characteristics when the tested module operates.

(3) One set includes 4 inner boxes and each inner box has 10 trays which contain 60 pieces of LCD modules each and an empty tray as the cover.

12. PRECAUTIONS IN DESIGN

12.1 GENERAL ATTENTION

(1) The LCD module covered by this specification has been designed specifically for a virtual reality application. When used for other applications, we do not warrant any of the content of these specifications including quality and safety sections. Furthermore, this module has not been explicitly developed for medical equipment critically related to human life such as life support apparatus.

(2) Never attempt to disassemble this LCD module. There is a danger of burns, electric shock, and injury. If the module is disassembled, we do not warrant any of these specifications including quality and safety sections.

12.2 PRECAUTIONS AGAINST ELECTROSTATIC DISCHARGE

This module includes C-MOS LSI(s), which are sensitive and vulnerable to electrostatic discharge. Any operator should be grounded with suitable anti-ESD equipment such as a wrist band when handling the module. Avoid touching terminal pins directly.

12.3 HANDLING PRECAUTIONS

(1) Do not subject the LCD module to a humid environment for any extended period. If the ambient storage temperature is over 35°C, steps should be taken to avoid high humidity. The polarizer can deteriorate under high temperatures and high humidity. Additionally, this can also cause the polarizer to bubble and peel. Please store/operate the LCD module within the specified temperatures and humidity ranges.

(2) As polarizer material tends to be easily scratched, the LCD module must be handled with due care to avoid touching, pressure or rubbing by any material which is harder than 3H pencil lead (e.g. metal fixings, tweezers, glass, etc.)

(3) No pressure more than 19.6 kPa must be applied to the LCD module surface. If pressure is exerted over an area of less than 1 cm^2, the maximum pressure must not exceed 1.96 N.

(4) As adhesives containing organic materials are used for securing upper and lower polarizers, these can be deteriorated by chemical reaction with chemicals such as acetone, toluene, ethanol and isopropyl alcohol (IPA). The following solvent is recommended for use : Normal hexane. Please contact us if it is necessary to use chemicals other than these mentioned above.

(5) Lightly wipe the surface with a clean, soft material such as a cotton swab or cleaning cloth for glasses, dampened with the recommended chemical. Always wipe the surface horizontally or vertically. Never wipe using a circular motion and avoid excess pressure or scrubbing. To prevent the display surface from damage and to maintain in a good state, it is generally sufficient, to wipe the surface with a cotton swab.

(6) If spittle or a water drop comes in contact with the display area, immediately wipe it off. Liquids can damage the LCD module resulting in deformation and faded color.

(7) Condensation on the LCD module may cause staining, dirtying or damage to the polarizer. If it is necessary to move the LCD module from an area of lower ambient temperature to a higher one, it is required to let it normalize to the new ambient temperature before unpacking or use.

(8) Touching the display area or the terminal pins with bare hands or contaminating them should be avoided. In our experience, staining on the display area and poor insulation between terminals are often caused by being touched with bare hands. (Some cosmetics are detrimental to polarizers.)

(9) As the display is made of glass, it is possible to break under shock loads, especially the periphery can be easily cracked or chipped in handling. Please handle the module with care and prevent it from being dropped.

(10) Never bend nor scratch the interface part. These actions can cause poor electrical contact.

(11) Since the top and bottom areas of bent FPC tend to be easily damaged, be very careful not to push or hold in those areas.

(12) Be careful not to apply local stress to the back of the LCD module. This will potentially cause scratching to the backlight guide, or result in a non-uniformity issue. Pay extra attention to the interface connector portion at the time of connector insertion.

(13) Never hold the LCD module by the FPC when handling.

(14) Please insert the FPC into the connector first, keeping the FPC parallel to the connector's opening. Be sure to lock the connector before securing the module.

12.4 OPERATION PRECAUTION

(1) Noise spikes can cause a malfunction of the circuit. Recommended condition of spike noise level is: Vcc = ±200 mV (over and under shoot voltage).

(2) Response time depends on temperature (at a lower temperature, it becomes longer). Brightness and color are also temperature dependant.

(3) Be aware of the possibility of condensation under a sudden temperature change. Formation of dewdrops can cause damage to polarizer or electrical contacts and result inferior displaying or malfunction. And even after the condensation has dispersed, smears or spots may occur on the display surface.

(4) When a fixed pattern is displayed for a long period, afterimage is likely to occur.

(5) As the LCD module provides a high frequency circuit, sufficient countermeasures against electromagnetic noise, such as shielding, may be required.

(6) Do not connect nor disconnect the module to or from main system with power applied.

(7) Provide light shielding so that the driver is not exposed to light. Exposure to strong light may cause malfunction of the driver.

12.5 STORAGE

When storing the LCD modules as spare parts, the following precautions are necessary.

(1) Store the LCD modules in a dark place; do not expose them to sunlight or fluorescent light. Keep the temperature between 10 and 30°C, and the humidity between 55% and 75%RH.

(2) The polarizer surface should not come in contact with any other object. It is recommended that the LCD modules are stored in the container in which they were shipped.

12.6 SAFETY

This LCD module is a glass product. In case of damage, ensure operators wear a pair of protective gloves whilst handling it. Additionally, if any liquid (liquid crystal) accidentally comes into contact with skin, immediately wash it off with soap and water.

12.7 MECHANICAL DESIGN

(1) The design of the HMD case and other components for this LCD module should be well studied so that any shock will not be transferred to the LCD module. When the HMD is dropped and the case provides insufficient shock absorption, the LCD module may become damaged.

(2) Providing a cushion material (e.g. PORON) in the case will help to reduce shock load transfer to the LCD driver.

(3) To prevent foreign substances from entering the display area, please apply a polyurethane foam cushion (e.g. PORON) around the LCD.

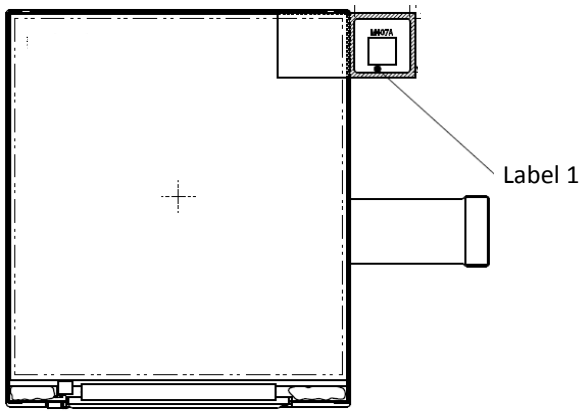
12.8 ENVIRONMENTAL PROTECTION

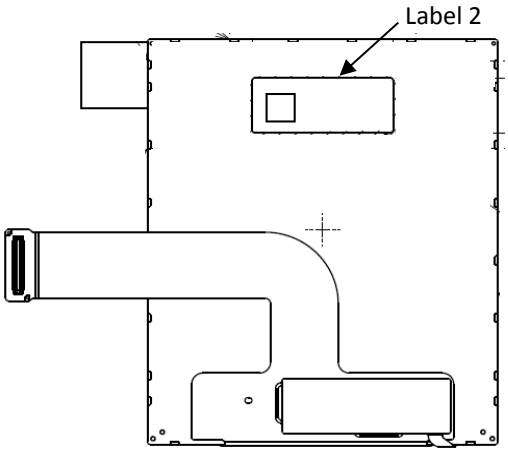
(1) Abide by national laws, legislation and local regulations when disposing of this LCD module.

(2) This LCD module complies with RoHS Directive.

13. LOT MARK

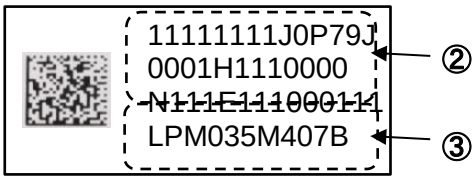
Lot mark is printed on the LCD module.





Label 1

Label 2



①：JDI Product Name (Last 5 digits)

②：JDI internal information

③：LPM035M407B

④

A 1 N 7 A 500001

⑤ ⑥ ⑦ ⑧ ⑨ ⑩

④：JDI Product Name

⑤：Revision

⑥：JDI Production Control No.

⑦：Production Base N：Nanox

⑧：Manufacturing date (Year)

Year	Figure in lot mark
2017	7
2018	8
2019	9
2020	0

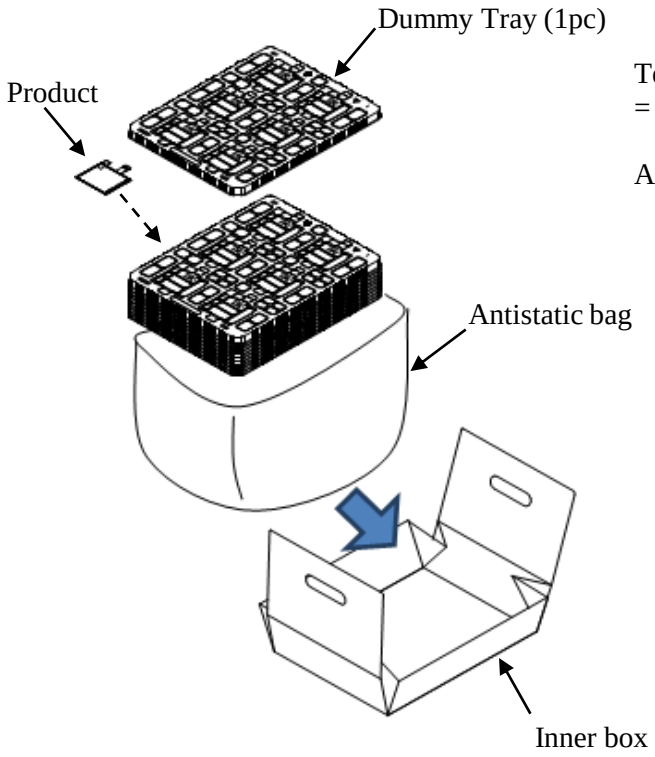
⑨：Manufacturing date (Month)

Month	Figure in lot mark	Month	Figure in lot mark
Jan.		July	
Feb.		Aug.	
Mar.		Sep.	
Apr.		Oct.	A
May		Nov.	B
June		Dec.	C

⑩：JDI Production Control No.

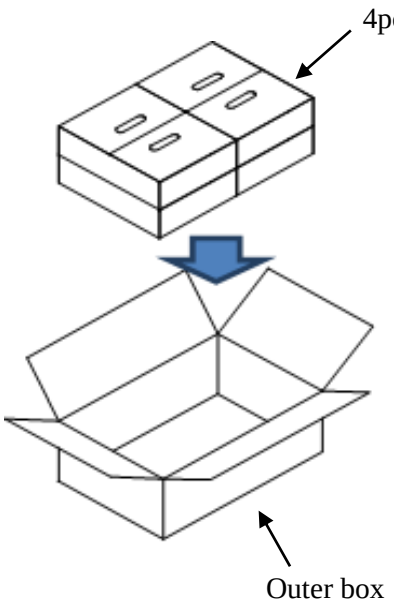
14. PACKING SPECIFICATIONS

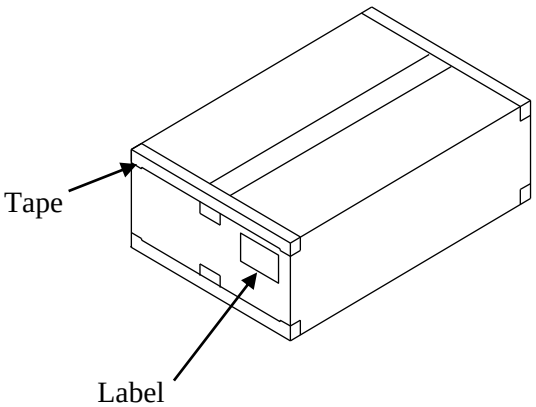
14.1 NANOX INNER BOX SPECIFICATIONS



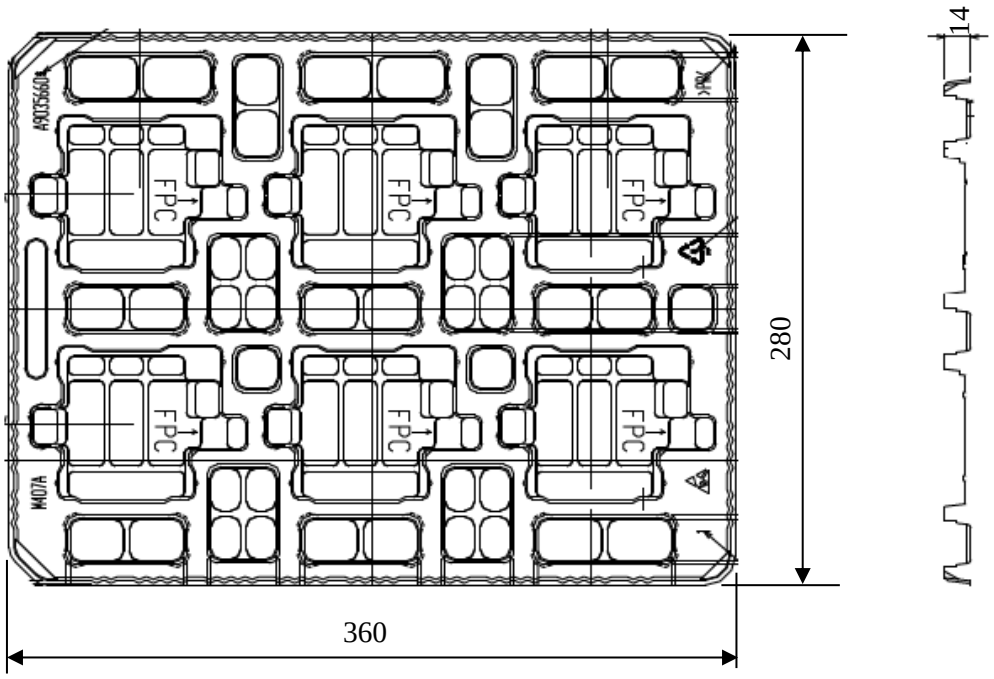
Ten (10) trays with products + empty tray as cover
= Eleven (11) trays (60 modules per batch)

As for all trays, stack up in the same direction.

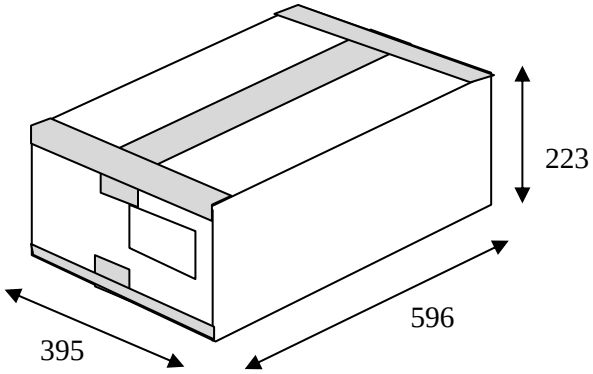




Size of Tray

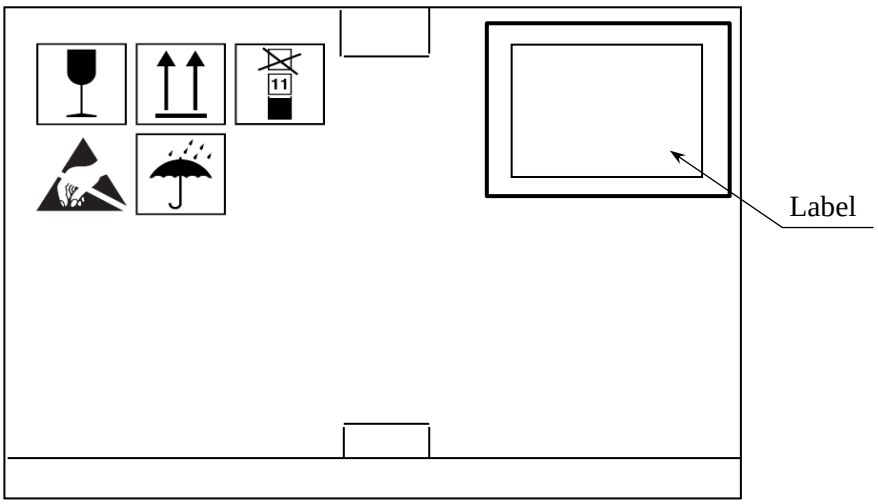


Size (L, W, H)	360 × 280 ×14 mm
Quantity	Max 6 pcs



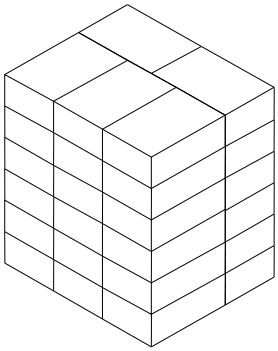
Size (L, W, H)	395 × 596 × 223 mm
Quantity	1 to 240 pcs

Marking on Outer Box (Example)

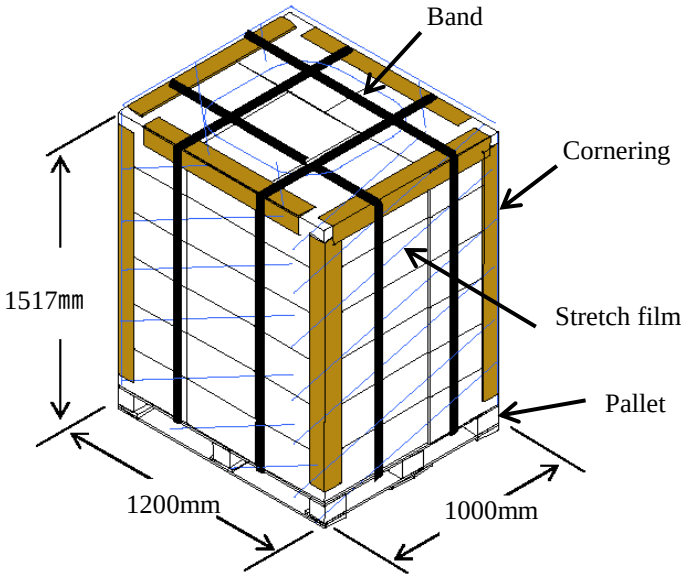


14.2 PALLET SPECIFICATIONS

Stacking pattern of outer box



5 boxes × 6 stacking



Weight (gross)	Approx.356 kg when the quantity is 7200 pcs
BOX quantity	30boxes (5 x 6)
Size (L, W, H)	1200×1000×1517mm
Quantity	Max 7200 pcs

14.3 Label detailed example

	Product code
	Product name
3	Date code (yyyy-mm-dd-0000)
	Quantity
	Country of production

15. PRECAUTIONS FOR USE

(1) A limit sample shall be provided by both parties when both parties agree to its necessity. Judgment by limit sample shall take effect after the limit sample has been established and confirmed by both parties.

(2) Under the following situations, handling of the problem should be decided through immediate discussion and agreement between responsible people of both parties.

a) When a question arises concerning the specifications.

b) When a new item which is not mentioned in the specification occurs.

c) When the customer changes any item of inspection specification or operating condition and reports it to Japan Display, and an issue with the specification arises because of this change.

d) When a new issue is found with the customer's operating set for sample evaluation.

(3) All the specifications in this document become effective immediately after approval signatures of both parties are in place.